AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (currently amended): A multiplexer structure comprising:

a semiconductor substrate having a shared diffusion region;

~~a first gate disposed on the shared diffusion region, the first gate having a first finger and a second finger;~~

~~a second gate disposed on the shared diffusion region, the second gate having a first finger and a second finger;~~

a contact for a first input node disposed on the shared diffusion region ~~between the first and second fingers of the first gate~~;

a contact for a second input node disposed on the shared diffusion region ~~between the first and second fingers of the second gate~~;

~~a contact~~ first, second and third contacts for a collector node disposed on the shared diffusion region; ~~between the first and second gates,~~

a first gate disposed on the shared diffusion region, the first gate having a first finger disposed between the contact for the first input node and the first contact for the collector node and a second finger disposed between the contact for the first input node and the second contact for the collector node; and

a second gate disposed on the shared diffusion region, the second gate having a first finger disposed between the contact for the second input node and the second contact for the collector node and a second finger disposed between the contact for the second input node and the third contact for the collector node, wherein

closing the first gate electrically connects the first input node and the collector node, and

closing the second gate electrically connects the second input node and the collector node.

Claim 2 (original): A multiplexer structure according to claim 1, wherein

the first gate, the first input node and the collector node define a first transistor element, and

the second gate, second input node and the collector node define a second transistor element.

Claim 3 (original): A multiplexer structure according to claim 1, further comprising:

a first memory element connected to the first gate for closing the first gate; and

a second memory element connected to the second gate for closing the second gate.

Claim 4 (original): A multiplexer structure according to claim 3, wherein a spacing between the first gate and the second gate is comparable to a linear dimension of the first memory element.

Claim 5 (original): A multiplexer structure according to claim 1, further comprising:

a first input element connected to the first input node for providing input values to the first input node; and

a second input element connected to the second input node for providing input values to the second input node.

Claim 6 (original): A programmable logic device, comprising: a multiplexer structure according to claim 1.

Claim 7 (original): A data processing system, comprising: a programmable logic device according to claim 6.

Claim 8 (currently amended): A multiplexer structure comprising:

a semiconductor substrate having a plurality of shared diffusion regions;

~~a plurality of gates disposed on the substrate across the shared diffusion regions, each gate having a first finger and a second finger;~~

a plurality of contacts for input nodes disposed on the shared diffusion regions ~~between the first and second fingers of the gates~~;

a plurality of contacts for collector nodes disposed on the shared diffusion regions ~~between the gates~~ ;and

a plurality of gates disposed on the substrate across the shared diffusion regions, each gate having a first finger and a second finger that enclose at least one of the input node contacts, and each two adjacent gates being separated by at least one of the collector node contacts, wherein closing a first gate electrically connects [[a]] corresponding input ~~node~~ nodes enclosed by the first gate with adjacent collector nodes in the shared diffusion regions.

Claim 9 (original): A multiplexer structure according to claim 8, wherein in each shared diffusion region a configuration of the first gate, an input node between the fingers of the first gate, and at least one collector node adjacent to the first gate defines a transistor element.

Claim 10 (original): A multiplexer structure according to claim 8, further comprising: a plurality of memory elements connected to the gates for closing the gates.

Claim 11 (original): A multiplexer structure according to claim 10, wherein a spacing between the gates is comparable to a linear dimension of the memory elements.

Claim 12 (original): A multiplexer structure according to claim 8, further comprising: a plurality of input elements connected to the inputs nodes for providing input values to the input nodes.

Claim 13 (original): A multiplexer structure according to claim 8, further comprising: a connecting element for electrically connecting the contacts of collector nodes across a first shared diffusion region so that the connecting element provides a multiplexer output from the input nodes in the first shared diffusion region.

Claim 14 (original): A multiplexer structure according to claim 8, further comprising: a plurality of connecting elements for electrically connecting the contacts of collector nodes across the shared diffusion regions so that the connecting elements provide a multiplexer output stage from the input nodes in the shared diffusion regions.

Claim 15 (original): A programmable logic device, comprising: a multiplexer structure according to claim 8.

Claim 16 (original): A data processing system, comprising: a programmable logic device according to claim 15.

Claim 17 (currently amended): A method of providing a multiplexing structure, comprising:

providing a semiconductor substrate having a shared diffusion region;

~~disposing a first gate on the shared diffusion region, the first gate having a first finger and a second finger;~~

~~disposing a second gate on the shared diffusion region, the second gate having a first finger and a second finger;~~

disposing a contact for a first input node on the shared diffusion region ~~between the first and second fingers of the first gate~~;

disposing a contact for a second input node on the shared diffusion region ~~between the first and second fingers of the second gate~~;

disposing ~~a contact~~ first, second and third contacts for a collector node on the shared diffusion region ~~between the first and second gates;~~

disposing a first gate on the shared diffusion region, the first gate having a first finger disposed between the contact for the first input node and the first contact for the collector node and a second finger disposed between the contact for the first input node and the second contact for the collector node; and

disposing a second gate on the shared diffusion region, the second gate having a first finger disposed between the contact for the second input node and the second contact for the collector node and a second finger disposed between the contact for the second input node and the third contact for the collector node, wherein

closing the first gate electrically connects the first input node and the collector node, and

closing the second gate electrically connects the second input node and the collector node.

Claim 18 (original): A method according to claim 17, wherein

the first gate, the first input node and the collector node define a first transistor element, and

the second gate, second input node and the collector node define a second transistor element.

Claim 19 (original): A method according to claim 17, further comprising:

connecting a first memory element to the first gate for closing the first gate; and

connecting a second memory element to the second gate for closing the second gate.

Claim 20 (original): A method according to claim 19, wherein a spacing between the first gate and the second gate is comparable to a linear dimension of the first memory element.

Claim 21 (original): A method according to claim 17, further comprising:

connecting a first input element to the first input node for providing input values to the first input node; and

connecting a second input element connected to the second input node for providing input values to the second input node.

Claim 22 (currently amended): A method of providing a multiplexer structure comprising:

providing a semiconductor substrate having a plurality of shared diffusion regions;

~~disposing a plurality of gates on the substrate across the shared diffusion regions, each gate having a first finger and a second finger;~~

disposing a plurality of contacts for input nodes on the shared diffusion regions ~~between the first and second fingers of the gates~~;

disposing a plurality of contacts for collector nodes on the shared diffusion regions ~~between the gates~~

disposing a plurality of gates on the substrate across the shared diffusion regions, each gate having a first finger and a second finger that enclose at least one of the input node contacts, and each two adjacent gates being separated by at least one of the collector node contacts, wherein closing a first gate electrically connects [[a]] corresponding input ~~node~~ nodes enclosed by the first gate with adjacent collector nodes in the shared diffusion regions.

Claim 23 (original): A method according to claim 22, wherein in each shared diffusion region a configuration of the first gate, an input node between the fingers of the first gate, and at least one collector node adjacent to the first gate defines a transistor element.

Claim 24 (original): A method according to claim 22, further comprising: connecting a plurality of memory elements to the gates for closing the gates.

Claim 25 (original): A method according to claim 24, wherein a spacing between the gates is comparable to a linear dimension of the memory elements.

Claim 26 (original): A method according to claim 22, further comprising: connecting a plurality of input elements to the inputs nodes for providing input values to the input nodes.

Claim 27 (original): A method according to claim 22, further comprising: providing a connecting element for electrically connecting the contacts of collector nodes across a first shared diffusion region so that the connecting element provides a multiplexer output from the input nodes in the first shared diffusion region.

Claim 28 (original): A method according to claim 22, further comprising: providing a plurality of connecting elements for electrically connecting the contacts of collector nodes across the shared diffusion regions so that the connecting elements provide a multiplexer output stage from the input nodes in the shared diffusion regions.

Claim 29 (new): A multiplexer structure comprising:

a semiconductor substrate having a plurality of shared diffusion regions;

a plurality of contacts for input nodes disposed on the shared diffusion regions;

a plurality of contacts for collector nodes disposed on the shared diffusion regions; and

a gate disposed on the substrate across the shared diffusion regions, the gate having a first finger and a second finger that enclose the input node contacts, wherein closing the gate electrically connects corresponding input nodes and collector nodes in the shared diffusion regions.

Claim 30 (new): A multiplexer structure according to claim 29, wherein in each shared diffusion region a configuration of the gate, an input node between the fingers of the gate, and at least one collector node adjacent to the gate defines a transistor element.

Claim 31 (new): A multiplexer structure according to claim 29, further comprising: a memory element connected to the gate for closing the gate.

Claim 32 (new): A multiplexer structure according to claim 29, further comprising: a plurality of input elements connected to the inputs nodes for providing input values to the input nodes.

Claim 33 (new): A programmable logic device, comprising: a multiplexer structure according to claim 29.

Claim 34 (new): A data processing system, comprising: a programmable logic device according to claim 33.

Claim 35 (new): A method of providing a multiplexer structure comprising:

providing a semiconductor substrate having a plurality of shared diffusion regions;

disposing a plurality of contacts for input nodes on the shared diffusion regions;

disposing a plurality of contacts for collector nodes on the shared diffusion regions;

disposing a gate disposed on the substrate across the shared diffusion regions, the gate having a first finger and a second finger that enclose the input node contacts, wherein closing the gate electrically connects corresponding input nodes and collector nodes in the shared diffusion regions.

Claim 36 (new): A method according to claim 35, wherein in each shared diffusion region a configuration of the gate, an input node between the fingers of the gate, and at least one collector node adjacent to the gate defines a transistor element.

Claim 37 (new): A method according to claim 35, further comprising: connecting a memory element to the gate for closing the gate.

Claim 38 (new): A method according to claim 35, further comprising: connecting a plurality of input elements to the inputs nodes for providing input values to the input nodes.